AMENDMENTS TO THE SPECIFICATION:

Please add the following new paragraph after the title of the invention on page 1, line 2:

This application is a divisional of Application No. 09/034,257, filed on March 4, 1998.

Please replace the paragraph beginning on page 1, line 26 and ending on page 2, line 24, with the following amended paragraph:

In FIG. 1, the reference number 1 designates a two-input NAND gate. Each of the reference numbers 2 and 3 denotes a p channel type metal oxide semiconductor field effect transistor (hereinafter referred to as a p MOS FET). Each of the reference numbers 4 and 5 indicates [[a]] n channel type metal oxide semiconductor field effect transistors (hereinafter referred to as a n channel MOS FET). In the circuit shown in FIG. 1, the absolute value of the threshold voltage of this p MOS FET is set to a low value and the absolute value of the threshold voltage of this n MOS FET is set to a high value. The reference number 6 designates a power source of a predetermined voltage, 7 denotes a ground power source. The reference number 8 indicates a p channel MOS FET connected between the power source 6 and a power source line 12 as a hypothetical power source line. This p channel MOS FET 8 becomes active when a gate terminal of the P channel MOS FET 8 receives a control signal 9. The reference number 10 indicates [[a]] an n channel MOS FET connected between [[the]] ground 7 and a ground line 13 that is a hypothetical ground line. This n channel MOS FET 10 becomes active when a gate

terminal of the n channel MOS FET 10 receives a control signal 11. In this circuit shown in FIG. 1, it is formed so that the absolute values of the threshold voltages of the p channel MOS FET 8 and the n channel MOS FET 10 are higher than the absolute values of the threshold voltages of the p channel MOS FETs 2 and 3 and the n channel MOS FETs 4 and 5 forming the two-input NAND gate 1, respectively.

Please replace the paragraph beginning on page 6, line 10 and ending on page 6, line 23, with the following amended paragraph:

Because the conventional circuit capable of performing under the low voltage as the semiconductor integrated circuit device has the configuration described above, namely, because both MOS FETs having the high threshold voltage and the low threshold voltage are formed in the array section 210, it is difficult to use the regions 260 (that is used for the MOS FETs having the high threshold voltage) in the array section for the internal circuits such as the two-input NAND gate 1 and wiring transferring signals and voltages of power source. Thereby, it becomes necessary to reduce the wiring efficiency in the array section 210 and the peripheral section thereof. This limitation causes to reduce the density of the layout of the semiconductor integrated circuit device.

Please replace the paragraph beginning on page 11, line 26 and ending on page 12, line 27, with the following amended paragraph:

The circuit capable of performing under the low voltage (hereinafter referred to as the low voltage operation circuit) comprises multi-threshold complementary metal oxide

semiconductors (hereinafter referred to as MT CMOS). In FIG. 1, the reference number 1 designates a two-input NAND gate, each of the reference numbers 2 and 3 denotes a p channel type metal oxide semiconductor field effect transistor (hereinafter referred to as a p MOS FET). Each of the reference numbers 4 and 5 indicates [[a]] n channel type metal oxide semiconductor field effect transistors (hereinafter referred to as a n channel MOS FET). The absolute value of the threshold voltage of this p MOS FET is set to a low value and the absolute value of the threshold voltage of this n MOS FET is set to a high value. The reference number 6 designates the power source, 7 denotes the ground power source. The reference number 8 indicates the p channel MOS FET connected between the power source 6 and a power source line 12 as a hypothetical power source line. This p channel MOS FET 8 becomes active when a gate terminal of the P channel MOS FET 8 receives the control signal 9. The reference number 10 indicates the n channel MOS FET connected between the ground power source 7 and the ground voltage line 13 that is a hypothetical ground line. This n channel MOS FET 10 becomes active when a gate terminal of the n channel MOS FET 10 receives the control signal 11. In this circuit shown in FIG. 1, it is formed so that the values of the threshold voltages of the p channel MOS FET 8 and the n channel MOS FET 10 are higher than the values of the threshold voltages of the p channel MOS FETs 2 and 3 and the n channel MOS FETs 4 and 5 forming the two-input NAND gate 1, respectively.

Please replace the paragraph beginning on page 12, line 28 and ending on page 13, line 13, with the following amended paragraph:

FIG. 3 is a diagram showing a layout pattern of the low voltage operation circuit shown in FIG. [[1]] 3 as the semiconductor integrated circuit device of the first embodiment according to the present invention. In FIG. 1, the reference number 21 designates an array section in which a plurality of MOS FETs are arranged in array form, 22 to 25 denote input/output circuit section in which input/output circuits are formed in peripheral regions in the array section 21. The reference number 27 indicates regions in which MOS FETs (high threshold voltage MOS FET) are formed in and each MOS FET in the regions 27 has a higher threshold voltage than the threshold voltage of each MOS FET formed in the array section 21. In the regions other than the regions 27 in the input/output circuit sections 22 to 25, input/output circuits are formed.

Please replace the paragraph beginning on page 19, line 8 and ending on page 19, line 25, with the following amended paragraph:

FIG. 6 is a diagram showing another layout pattern of the low voltage circuit capable of performing under the low voltage as the semiconductor integrated circuit device of the second embodiment according to the present invention. In FIG. 6, each of the input/output circuit forming regions 221, 231, 241, and 251 is made up of a plurality of regions. In each of the regions 221, 231, 241, and 251, both MOS FETs having a low threshold voltage (hereinafter, also referred to as low threshold voltage MOS FET) and MOS FETs having a high threshold voltage (hereinafter, also referred to as high threshold

voltage MOS FET) are formed. Each of the regions 221, 231, 241, and 251 is the same configuration in the semiconductor integrated circuit as the ~~second~~ first embodiment. The reference numbers 51 to 54 designate regions in the regions 221, 231, 241, and 251 in which the high threshold voltage MOS FETs are formed. In FIG. 6, the regions 51 to 54 are designated by shadowed lines or slanted lines.

Please replace the paragraph beginning on page 22, line 7 and ending on page 22, line 18, with the following amended paragraph:

FIG. 8 is a diagram showing another layout pattern of the low voltage circuit capable of performing under the low voltage as the semiconductor integrated circuit device as the third embodiment according to the present invention. In FIG. 8, the reference numbers 71, 72, 73, and 74 designate space areas located at four corners of the array section 21 other than the input/output circuit forming regions 22, 23, 24, and 25 in a semiconductor chip. In this third embodiment, the high threshold voltage MOS FETs are formed at the space areas 71 to 74 in the four corners. In FIG. 8, the space areas ~~55, 56, and 57~~ are designated by shadowed lines or slanted lines.

Please replace the paragraph beginning on page 23, line 11 and ending on page 23, line 20, with the following amended paragraph:

FIG. 9 is a diagram showing another layout pattern of the low voltage circuit capable of performing under the low voltage as the semiconductor integrated circuit device of the fourth embodiment according to the present invention. In FIG. 9, the reference number 75 designates a space area located between the array section 21 and the input/output circuit forming areas 22 to 25. In FIG. 9, the space area [[71]] 75 is designated by shadowed lines or slanted lines. In the space area 75, the MOS FETs having the high threshold voltage are formed.